Q.P. Code: 20EC4202 **R20**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

MTECH I Year I Semester Regular Examinations July-2021

DIGITAL IC DESIGN

(VLSI)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Draw the circuit for NMOS inverter and explain its operation.	L1	**6M**
	b	Draw the ideal characteristics of a CMOS inverter and compare it with the actual characteristics.	L1	**6M**
		OR		
2	a	Implement the 2-input NAND gate with CMOS logic and explain its working.	L6	**6M**
	b	Discuss about the performance of dynamic CMOS inverter.	L6	**6M**
		UNIT-II		
3	a	Sketch the schematic diagram of a SRAM memory cell along with sense amplifier and data write circuitry.	L1	**6M**
	b	Why low power has become an important issue in the present day VLSI circuit realization?	L1	**6M**
		OR		
4	a	Explain how read and write operations are performed in a SRAM.	L2	**6M**
	b	Discuss about power consumption in CMOS gates.	L6	**6M**
		UNIT-III		
5	a	Explain in detail how do we calculate power for Bi-CMOS and on what parameters the power equation depends on?	L2	**8M**
	b	List the advantages and disadvantages of Bi-CMOS.	L4	**4M**
		OR		
6	a	Compare the switching characteristics of a Bi-CMOS inverter with respect to that for static CMOS for different fan out conditions.	L2	**4M**
	b	Draw the schematic diagram of different Bi-CMOS inverters. Explain its operation.	L1	**8M**
		UNIT-IV		
7	a	What is the need for design rules? Explain.	L1	**4M**
	b	Write about: (i) Area capacitance (ii) Drive large capacitive load	L1	**6M**
		OR		
8	a	Explain two input NAND gate with relevant Layout example.	L2	**6M**
	b	What are the CMOS based design rules?	L1	**6M**
		UNIT-V		
9	a	Explain Booth's algorithm and its modified algorithm.	L2	**6M**
	b	Discuss about design approach of carry look ahead adder with neat sketch.	L6	**6M**
		OR		
10	a	Discuss about design approach of 4-bit shifter.	L6	**6M**
	b	Design a 4-bit CLA adder.	L6	**6M**

*** END ***